CBCS SCHEME

USN | | | | | | | | | | **17EE35**

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high. Use K_{map} to simplify. **(10 Marks)**

b. Using K_{maps}, simplify,

$$S = \overline{A}B\overline{C} + A\overline{B}\,\overline{C}D + ABCD + ABC\overline{D} + AB\overline{C}\,\overline{E} + ABCE + d(A\overline{B}C\overline{D} + \overline{A}BCE).$$ **(10 Marks)**

OR

2 a. Simply the following function using Quine Mc-Cluskey method.
$P = f(w, x, y, z) = \Sigma m(1, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$. **(10 Marks)**

b. Explain with suitable examples :
i) How do we obtain a standard SOP expression from a SOP expression?
$y = AB + BC + AC$.
ii) How do we obtain a standard POS expression from a POS expression?
$y = (A + B)(B + C)(A + C)$. **(10 Marks)**

Module-2

3 a. Implement the function using active low output dual 2 : 4 line decoder IC 74139.
i) $f_1(P, Q, R) = \Sigma m(1, 4, 5, 7)$
ii) $f_2(P, Q, R) = \pi m(0, 1, 2, 6)$. **(08 Marks)**

b. Design a half and full subtractor and draw using NAND gates only. **(12 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \Sigma m(4, 5, 7, 10, 11, 12, 15)$ using :
i) 8 : 1 MUX with b, c, d as select lines
ii) 4 : 1 MUX with a, d as select lines. **(10 Marks)**

b. Write a truth table for two-bit magnitude comparator. Write the K – Map for each output of two bit magnitude comparator and the resulting equation. **(10 Marks)**

Module-3

5 a. Explain with timing diagrams the workings of SR latch as a switch debouncer. **(08 Marks)**

b. Draw the master Q and $\overline{Q}$ and slave Q and $\overline{Q}$ waveforms for J and K shown in Fig.Q5(b). **(12 Marks)**

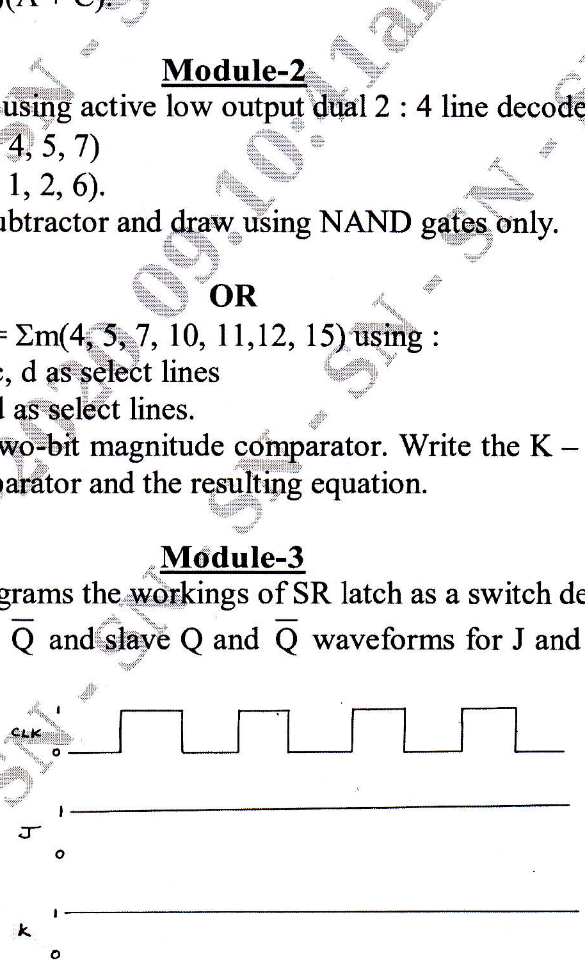

Fig.Q5(b)

OR

6 a. Design a 4 bit shift register using positive edge triggered Dflip-flops to operate as indicated in the table below.

Mode select		Register operation
S_1	S_0	
0	0	Hold
0	1	Clear counter
1	0	Complement contents
1	1	Circular shift right

(10 Marks)

b. Design a Mod-6 ripple counter using clocked T flip-flops. (10 Marks)

Module-4

7 a. Explain mealy model and Moore model in detail with necessary block diagrams. (08 Marks)

b. Analyse the following sequential circuit shown in Fig.Q7(b) and obtain :
   i) Flip flop input and output equations
   ii) Transition equation
   iii) Transition table
   iv) State table
   v) State diagram.

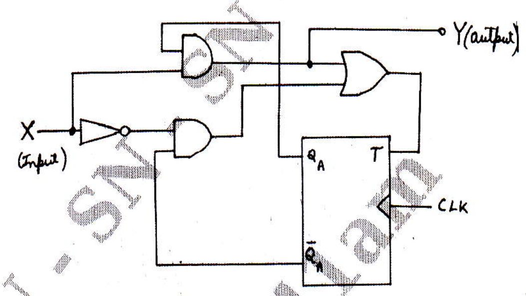

Fig.Q7(b)

(12 Marks)

OR

8 a. For the state diagram shown in Fig.Q8(a), design a sequential circuit using Dflip-flop. (10 Marks)

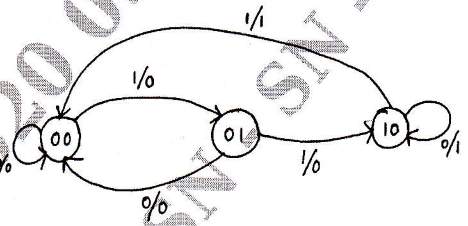

Fig.Q8(a)

b. Design a synchronous counter using Negative edge triggered Dflip-flop having the sequence : 1 – 6 – 12 – 10 – 5 – 3 – 7 – 2 – 13 – 4 – 1. (10 Marks)

Module-5

9 a. Explain briefly the structure of the VHDL module. (10 Marks)

b. Briefly explain the operators in VHDL. (10 Marks)

OR

10 a. For a 2 × 1 multiplexer with active low enable, write a VHDL dataflow description and verilog description. (12 Marks)

b. Give the comparison between concurrent and sequential signal assignment statements. (08 Marks)

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